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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,899	08/06/2003	Nhon T. Quach	02207/868702	7340

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EXAMINER	
IQBAL, NADEEM	
ART UNIT	PAPER NUMBER
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/634,899	QUACH ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 7-22* is/are rejected.

7)☒ Claim(s) *3-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 7 recites the limitation "the result latch" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claims 1-3 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 6654909. This is a double patenting rejection.

3. Claim 4 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 2 of prior U.S. Patent No. 6654909. This is a double patenting rejection.

4. Claims 5-8 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 3-6 of prior U.S. Patent No. 6654909. This is a double patenting rejection.

5. Claims 9 & 10 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 8 of prior U.S. Patent No. 6654909. This is a double patenting rejection.

6. Claims 11-16 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 9-14 of prior U.S. Patent No. 6654909. This is a double patenting rejection.

7. Claims 17, 18 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 14 of prior U.S. Patent No. 6654909. This is a double patenting rejection.

8. Claims 19-22 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 16-19 of prior U.S. Patent No. 6654909. This is a double patenting rejection.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 17 is rejected under 35 U.S.C. 101 because the claim recites "comprising a computer-readable medium". A correction is need to overcome this rejection by inserting word "storage" after "computer-readable".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 2, 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Godiwala et al., (U.S. Patent number 5361267).

4. As per claim 1, Godiwala et al., teaches (col. 3, lines a computer system where all read transactions are checked for errors and upon recognition of such errors, the errors are promptly reported to the processor. He also teaches (col. 4, lines 6-8) that errors are checked that include parity errors and hard errors. He also teaches (Abstract, lines 5-9) a control logic that include error checker to check for hard errors and parity errors and ECC generator to generate ECC. He thus teaches limitations pertain to an error detection component. With reference to a comparison component configured to receive information from the processor to determine if the information is valid and to output a signal to indicate an error condition. He teaches (Abstract, lines 10-12) an error signal generator that generates and transmits an error signal when there is a hard error or a parity error. He does not explicitly discloses a comparison component that determines if the information is valid. It would have been obvious to a person of ordinary skill in the art at the

time the information is made to realize that his error checker would include a comparison component. This is because He teaches detection for errors and generates an error signal upon detection of error in the received data, requiring a comparison component.

5. As per claim 2, With reference to the error detection component comprising an error detection state machine and outputs a next-to-read-out signal. He teaches (col. 3, lines 52-55).

6. As per claim 8, With reference to a cache, TLB, RID, MSR, CRAB, & TLB, Godiwala teaches the limitations (See Fig. 3).

7. As per claims 9 & 10, With reference to the CRAB includes at least one MSR coupled to the CRAB. Godiwala teaches as stated per claim 1 above, the control logic includes error checker to check for hard errors and parity errors and ECC generator to generate EC, therefore would include checksum component and the MSR components.

8. As per claim 11, Godiwala substantially teaches the claimed invention as discloses related to claim 1 above. He also teaches (col. 4, lines 6-8) that errors are checked that include parity errors and hard errors. He also teaches (Abstract, lines 5-9) a control logic that include error checker to check for hard errors and parity errors and ECC generator to generate ECC. He thus teaches limitations pertain to computing a parity bit value. With reference to a comparison component configured to receive information from the processor to determine if the information is valid and to output a signal to indicate an error condition. He teaches (Abstract, lines 10-12) an error signal generator that generates and transmits an error signal when there is a hard error or a parity error. He does not explicitly discloses a comparison component that determines if the information is valid. It would have been obvious to a person of ordinary skill in the art to realize that his error checker would include a comparison component. This is because He teaches

detection for errors and generates an error signal upon detection of error in the received data, requiring a comparison component.

9. As per claims 12 & 15, With reference to outputting a next-entry-to-read out signal. He teaches ((Abstract, lines 10-12, col. 3, lines 52-55).

10. As per claims 13 & 14, With reference to receiving a periodic read authorization signal and determining if the processor resource is in use. He teaches (col. 6, lines 16-20).

11. As per claims 15 & 16, With reference to outputting a signal to indicate an error condition and outputting a machine check abort signal. He teaches (Abstract, lines 10-12).

12. As per claim 17, Godiwala substantially teaches the claimed invention as discloses related to claim 11 above. He also teaches (col. 4, lines 6-8) that errors are checked that include parity errors and hard errors. He also teaches (Abstract, lines 5-9) a control logic that include error checker to check for hard errors and parity errors and ECC generator to generate ECC. He thus teaches limitations pertain to computing a parity bit value. With reference to a comparison component configured to receive information from the processor to determine if the information is valid and to output a signal to indicate an error condition. He teaches (Abstract, lines 10-12) an error signal generator that generates and transmits an error signal when there is a hard error or a parity error. He does not explicitly discloses a comparison component that determines if the information is valid. It would have been obvious to a person of ordinary skill in the art to realize that his error checker would include a comparison component. This is because He teaches detection for errors and generates an error signal upon detection of error in the received data, requiring a comparison component.

13. As per claim 18, With reference to outputting a next-entry-to-read out signal. He teaches ((Abstract, lines 10-12, col. 3, lines 52-55).

14. As per claims 19 & 20, With reference to receiving a periodic read authorization signal and determining if the processor resource is in use. He teaches (col. 6, lines 16-20).

15. As per claims 21 & 22, With reference to outputting a signal to indicate an error condition and outputting a machine check abort signal. He teaches (Abstract, lines 10-12).

16.

Allowable Subject Matter

17. Claims 3-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI